REMARKS

Applicant is in receipt of the Office Action mailed June 20, 2006. Claims 1-50 are pending in the case. Reconsideration of the present case is earnestly requested in light of the following remarks.

Double Patenting Rejections

Claims 1-50 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-59 of U.S. Patent No. 6,219,628 B1 to Kodosky et al. ("Kodosky"), in view of US Patent 5,005,119 to Rumbaugh et al. ("Rumbaugh").

Applicant has filed herewith a Terminal Disclaimer with respect to Kodosky, thus rendering the obviousness-type double patenting rejection moot, and respectively requests removal of the obviousness-type double patenting rejection of claims 1-50.

Section 103 Rejections

Claims 1, 3-21, 23-41, and 43-50 were rejected under 35 U.S.C. 103(a) as being unpatentable over WO 94/15311 to Duncan ("Duncan"), in view of "A Software Development System for FPGA-Based Data Acquisition Systems" by Alan Wenban and Geoffrey Brown ("Wenban").

Claim 1 recites:

1. A method for configuring a reconfigurable system, the method comprising:

displaying a graphical user interface on a display which is useable for configuring the reconfigurable system, wherein the reconfigurable system comprises a programmable hardware element and one or more fixed hardware resources coupled to the programmable hardware element, and wherein the graphical user interface displays fixed hardware resource icons corresponding to each of at least a subset of the one or more fixed hardware resources;

receiving user input to the graphical user interface specifying a function;

generating a hardware configuration program based on the user input, wherein the hardware configuration program is deployable on the reconfigurable system; and

deploying the hardware configuration program on the programmable hardware element, wherein the hardware configuration program specifies use of one or more of the fixed hardware resources;

wherein, after said deploying, the reconfigurable system is operable to perform the function.

The Examiner asserts that Duncan and Wenban teach all of the features and limitations of claim 1. Applicant respectfully disagrees.

The Examiner asserts that Duncan teaches fixed hardware resources as claimed, citing p.3:13, and p.4:1-5. More specifically, the Examiner asserts that Duncan's "underlying circuit design", represented by an icon, is a "fixed hardware resource". However, Applicant submits that Duncan's underlying circuit designs are selectable modular circuit designs representing components that may then be implemented on a programmable logic device, such as an FPGA (or on a custom IC). In other words, the icons represent modular *designs*, or *schematic* components, not actual existing physical components coupled to a programmable hardware element. In fact, the cited p.3:13 reads "Schematic designs are *descriptions* of the physical components and interconnections of a circuit" (emphasis added). Similarly, p.4:1-5 reads: "A schematic component is comprised of two parts: a schematic symbol (icon) which is displayed on a video monitor, and an underlying circuit design which defines the function of the schematic component". Clearly, a circuit *design* is not the same as the physical component itself. Thus, a circuit design is not itself a fixed hardware resource, since it is not hardware.

Applicant respectfully notes that, as the name clearly indicates, "fixed hardware resources" refer to those *hardware components* that are *fixed*, i.e., that are *already* present and coupled to an existing programmable hardware element, *not* to components that are implemented, or targeted for implementation, by the programmable hardware element. In other words, in Applicant's invention, the programmable hardware element may be configured to *use* the fixed hardware resources coupled to it, but does *not* implement them, as they are already there. Moreover, a component that is implemented in

programmable hardware, and thus, that can be reconfigured or removed, is not a *fixed hardware component*. Applicant respectfully submits that the Examiner has improperly equated Duncan's iconically represented schematic design elements (maintained in Duncan's library) with Applicant's actual physical fixed hardware resources coupled to the programmable hardware element, where the former *represents* hardware, and the latter *is* hardware. This is analogous with equating a *map* with the *territory* it describes.

The Examiner asserts that Duncan discloses "displaying a graphical user interface on a display which is useable for configuring the reconfigurable system, wherein the graphical user interface displays fixed hardware resource icons corresponding to each of at least a subset of the one or more fixed hardware resources", citing Duncan page 12, lines 20-23 and page 56, lines 6-7.

Applicant submits that the cited text actually discloses the use of a library of icons representing simple designs for inclusion in a circuit design, i.e., a schematic diagram. Duncan nowhere discloses a reconfigurable system comprising a programmable hardware element and *one or more fixed hardware resources coupled to the programmable hardware element*. In fact, as discussed above, Duncan fails to mention or even hint at fixed hardware resources at all.

Rather, in Duncan's system, once the schematic diagram (circuit design) has been specified, including the various components represented by the selected symbols/icons, it is used to generate a netlist. As Duncan describes in p.2:36 – p.3:2, a netlist is "usable either to produce a custom IC or to configure a programmable logic device". Thus, with regards to configuring a programmable logic device, e.g., a programmable hardware element, any component designs selected for inclusion in the schematic diagram are in fact implemented on the programmable logic device, and are specifically *not fixed hardware resources coupled to the programmable hardware element*. In other words, Duncan is directed to creating a circuitry design for subsequent implementation, e.g., on a programmable logic device (or as a custom integrated circuit), and neither mentions nor even hints at fixed hardware resources that are already coupled to a programmable hardware element, nor specifying functionality of a reconfigurable system that includes a programmable hardware element and one or more fixed hardware resources coupled to

the programmable hardware element via a GUI that displays icons representing those fixed hardware resources.

Nowhere does Duncan disclose a graphical user interface that displays *fixed hardware resource icons corresponding to each of at least a subset of the one or more fixed hardware resources*. As discussed above regarding the Examiners assertion that Duncan's "underlying circuit design", represented by an icon, is a "fixed hardware resource", Duncan's underlying circuit designs are selectable modular circuit designs *representing* components that may then be implemented on a programmable logic device, such as an FPGA (or on a custom IC). In other words, the icons represent modular *designs, or schematic components*, not actual existing hardware components coupled to a programmable hardware element.

In the Examiner's Response, the Examiner again asserts that Duncan's underlying circuit designs are fixed hardware resources, and thus that Duncan's schematic component library actually contains fixed hardware resources. However, as Applicant showed above, Duncan's library contains *schematic components* that *represent* various circuit components, such as counters, etc., which are displayed, and are selectable by the user for inclusion in a *circuit design*, which may (or may not) be subsequently implemented in a programmable logic device (or custom IC). Applicant notes that a circuit design for a counter is not an actual hardware counter, and more specifically, is not a counter already coupled to a programmable hardware element.

Thus, even after being included in the schematic diagram, Duncan's underlying circuit designs are neither *fixed*, nor actual *hardware resources*. Thus, Duncan's user interface does not display icons representing fixed hardware resources coupled to the programmable hardware element.

Thus, Duncan fails to teach or suggest this feature of claim 1.

The Examiner admits that Duncan fails to teach "deploying the hardware configuration program on the programmable hardware element, wherein the hardware configuration program specifies use of one or more of the fixed hardware resources", but asserts that Wenban remedies this citing page 36, #2 and #3. Applicant submits that the cited text actually describes a method by which an FPGA could be reconfigured using a

boot-strap loading of the reconfiguration data stored within on-board SRAM. Neither Wenban nor Duncan discloses any method for deploying the hardware configuration program on the programmable hardware element, wherein the hardware configuration program *specifies use of one or more of the fixed hardware resources*.

In the Examiner's Response, the Examiner asserts that "the design created by Duncan does specify 'fixed hardware resources' such as a counter". There are several problems with this assertion. For example, Applicant notes that a design *specifying* a counter for implementation on an FPGA is not the same as a design specifying *use* of a *fixed* counter that is already coupled to an FPGA. Furthermore, as noted above, Duncan's specified counter is not actualized until it is implemented, e.g., on a programmable logic device, which may or may not happen. In other words, a *specification* for a counter is *not* itself a hardware counter. Moreover, even if Duncan's specified counter *is* implemented on a programmable logic device, such as an FPGA, it will still not be a *fixed hardware resource*, as claimed. Applicant reminds the Examiner that the fixed hardware resources as claimed are *already* coupled to the programmable hardware element, and so do not refer to components that are implemented on the programmable hardware element. In other words, as argued previously, schematic components, i.e., software components representing circuitry, that are implemented on a programmable hardware element, are not fixed hardware resources that are already coupled to the programmable hardware element.

Thus, Wenban fails to remedy this admitted deficiency of Duncan.

Regarding the Examiner's combination of Duncan and Wenban, Applicant notes that Wenban's "more specific example" of deploying programmable code onto an FPGA does not disclose aspects of the present invention related to fixed hardware resources, as recited in claim 1. In fact, neither Wenban nor Duncan mentions these claimed features, and further, neither reference indicates or even hints at the desirability of these features. Thus, as argued at length above, even in combination, Duncan and Wenban would still not produce Applicant's invention as represented in claim 1.

Thus, for at least the reasons provided above, Applicant respectfully submits that Duncan and Wenban, taken singly or in combination, fail to teach all the features and limitations of claim 1, and so Applicant submits that claim 1 and those claims dependent therefrom are patentably distinct and non-obvious over the cited art, and are thus allowable.

Claims 11, 13, 21, 31, 33, and 41 include similar limitations as claim 1, and so the above arguments apply with equal force to these claims. Thus, for at least the reasons provided above, Applicant submits that claims 11, 13, 21, 31, 33, and 41, and those claims respectively dependent therefrom, are patentably distinct and non-obvious, and are thus allowable.

Applicant respectfully requests removal of the section 103 rejection of claims 1, 3-21, 23-41, and 43-50.

Claims 2, 22, and 42 were rejected under 35 U.S.C. 103(a) as being unpatentable over Duncan in view of Wenban in further view of Rumbaugh.

Applicant notes that if an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). The respective independent claims from which claims 2, 22, and 42 respectively depend have been shown above to be patentably distinct and non-obvious, and thus allowable, and so their respective dependent claims are similarly allowable, for at least the reasons provided above.

Thus, Applicant respectfully requests removal of the section 103 rejection of claims 2, 22, and 42.

Applicant also asserts that numerous ones of the dependent claims recite further distinctions over the cited art. However, since the independent claims have been shown to be patentably distinct, a further discussion of the dependent claims is not necessary at this time.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above-referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. The Commissioner is hereby authorized to charge any fees which may be required or credit any overpayment to Meyertons, Hood, Kivlin, Kowert & Goetzel P.C., Deposit Account No. 50-1505/5150-63500/JCH.

Also filed herewith is the following item:

☒ Terminal Disclaimer

Respectfully submitted,

/Jeffrey C. Hood/

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